The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A die-level opto-electronic device, comprising:

a semiconductor die having edges and a photonic device optically exposed on a first surface;

a conductive structure formed in and through at least a portion of the die and not on ~~away from~~ the side edges of the die, the conductive structure being exposed on a second surface of the die that opposes the first surface, wherein the conductive structure is electrically connected to the photonic device; and

an optically transparent laminate attached to the first surface so as to overlay the photonic device.

2. (Original) The die-level opto-electronic device of claim 1 wherein the photonic device is an image sensor.

3. (Original) The die-level opto-electronic device of claim 1 further comprising an under bump metallization pad attached to the second surface, the under bump metallization pad being electrically connected to the conductive structure.

4. (Original) The die-level opto-electronic device of claim 3 wherein the under bump metallization pad is redistributed so as to occupy a different location on the second surface than the conductive structure.

5. (Original) The die-level opto-electronic device of claim 1 further comprising a solder bump deposited on the conductive structure so as to extend beyond the second surface.

6. (Original) The die-level opto-electronic device of claim 1 wherein the optically transparent laminate comprises a glass.

7. (Currently Amended) A semiconductor wafer, comprising:

a substrate having a plurality of photonic devices optically exposed on a first surface;

a plurality of conductive structures formed in and through at least a portion of the substrate, the plurality of structures being exposed on a second surface of the substrate that opposes the first surface, wherein ones of the plurality of structures are electrically connected to associated ones of the plurality of photonic devices; and

an optically transparent laminate attached to the first surface so as to overlay the plurality of photonic devices.

8. (Original) The semiconductor wafer of claim 7 wherein the plurality of photonic devices further comprises a plurality of image sensors.

9. (Original) The semiconductor wafer of claim 7 further comprising a plurality of under bump metallization pads attached to the second surface, ones of the plurality of under bump metallization pads being electrically connected to associated ones of the plurality of conductive structures.

10. (Original) The semiconductor wafer of claim 9 wherein the plurality of under bump metallization pads is redistributed so as to occupy different locations on the second surface than the plurality of conductive structures.

11. (Original) The semiconductor wafer of claim 7 further comprising a plurality of solder bumps, wherein ones of the plurality of solder bumps are deposited on associated ones of the plurality of conductive structures so as to extend beyond the second surface.

12. (Original) The semiconductor wafer of claim 7 wherein the optically transparent laminate comprises a glass.